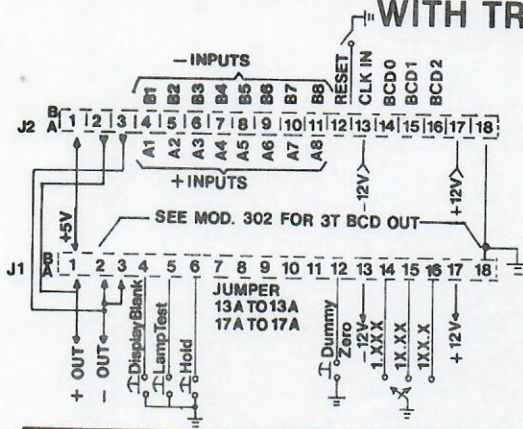




HI-REL ±3½ DIGIT 8 CHANNEL DIFFERENTIAL ANALOG MULTIPLEXING DPM WITH TRISTATE BCD OUTPUT

MODEL 320



FEATURES

- "3T" BCD Parallel Buffered
- Sequential Address
- Random Address
- ±10V CMV
- Conditioned Analog Output
- One Instrument Can Measure 8 Signals



DESCRIPTION

Using the Model 300 Main Frame as the basic instrument, the 320 can measure 8 different Analog Signals (one at a time) either Sequentially by applying a clock pulse to step its Internal Decoder or Randomly by addressing its BCD Inputs when so ordered.

The Analog Multiplexer IC is of the break before make type eliminating shorting problems and at its output a Differential Amplifier converts the Differential Signal to single ended for the A-D Section of the 300 Main Frame. This signal is available at the edge connector for external use and can supply up to 1mA Dc. All Digital Inputs/Outputs are TTL Compatible.

TERMINAL DESCRIPTION

Due to the number of channels offered, the 320 uses two Main Boards, the 300 Main Frame and the Analog Multiplexer Board. Due to this configuration, the Model 320 can offer Full Parallel "3T" BCD as an option; but, it must be powered by 5Vdc or External 115/230 Vac Power Supply. The 320 has two 36 Pin Connectors. J1 is the Main Frame Connector and J2 is the Analog Multiplexer Connector.

J1 Connections: (Bottom)

1B (Top) +5Vdc Input; 18B, Digital Ground (5V Return) 1A Bottom) + Signal Input from 2A of J2; 2A - Signal Input from 3A of J2 (connected internally to 18B). **Do not** allow power currents to flow on this line or **Offsets** (Ground Loops) will occur.

4A, Display Blank; 5A, Lamp Test; 6A, Display Hold (optional); 13A, -12Vdc out to 13A of J2; 14A, 1XX.X D.P.; 15A, 1X.XX D.P.; 16A, 1.XXX D.P. (connect to 18B to Light Up); 17A, +12Vdc out to 17A of J2; 18A, Sign Out (Low for +, High for -).

Pins 3 and 4B, OD1 and OD2 connect to Ground (18A) for normal operation connect +5V to force the BCD Output to Hi Z State; 5B thru 17B, BCD out as per label (See Model 302 on page 17). **Note:** Sign Pin 18A is not tristated. Ground 12A to activate Dummy Zero.

J2 Connections: (Top)

1A +5Vdc; 18A Digital Ground; 13A (-12V) connect to 13A of J1; 17A (+12V) connect to 17A of J1; 2A + Signal Out connect to 1A of J1; 3A - Signal Out connect to 2A of J1; 4A-11A (+ Signal In) Channels 1-8; 4B-11B (- Signal In) Channels 1-8; **Maximum Voltage Across Any Of These Pins Or To Digital Ground Should Not Exceed ±10Vdc.** 12B Reset a Logic "0" (Ground) at this pin will clear the Decoder and force the Multiplexer to "All Open" Condition, connect to +5V for normal operation; 13B Clock, a "1" to "0" transition will advance the Multiplexer to the next channel; 14B (BCD 0); 15B (BCD 1) 16B (BCD 2) used as Address Inputs. If Random Model is used or as Outputs is Sequential Type is ordered.

Note: Connectors Included

SPECIFICATIONS

Linearity	0.1%
Common Mode Voltage	10Vdc or AC
Maximum Input Voltage	±10V
Input Impedance	10 Mega OHMS
Common Mode Rejection	90dB @ 50-60 Hz
Clock and Reset Logic	1 Low Power TTL
No. of Channels	8
Analog Output	0.1mV or 1mV/Count, 1mA max.
Power Consumption	5Vdc @ 330mA
Polarity	Automatic
Zero	Automatic
Operating Temperature	-10 to +55°C
Storage Temperature	-20 to +70°C
Temperature Coefficient	±50PPM/°C
Input Ranges	+200mV and ±2.0V F.S.
Switching Type	Break Before Make

		Truth Table	
LEVEL	RPM	BCD	Reset Channel
CMV CH1	CH2	X	0 None
4A 4B	5A 5B	000	1 1
1A 8 CH. ANALOG MULTIPLEXER 2A	10A 10B	001	1 2
16A BOARD NO. 320	11A 11B	010	1 3
18B SERIES A300 WITH	3A	011	1 4
18 PAR. BCD & AN. MUX.	1A	100	1 5
13B 12B		101	1 6
TPAR BCD	PRINT	110	1 7
CLK RESET	IMC MOD	111	1 8
LOW COST	NP-7A		
DATA LOGGER WITH FLOATING INPUTS	CHANNEL BCD DATA		

ORDERING INFORMATION

MODEL 320 X X X

Range/Address/3TBDCD

0 ... 200mV/Random/No BCD
1 ... 2V/Random/No BCD
2 ... 200mV/Sequential/No BCD
3 ... 2V/Sequential/No BCD
4 ... 200mV/Random/BCD
5 ... 2V/Random/BCD
6 ... 200mV/Sequential/BCD
7 ... 2V/Sequential/BCD

Power

0 ... 5Vdc Req'd
1 ... Open Frame P.S.
2 ... Power Pack P.S.

Display

0 ... Standard
1 ... Dummy Zero

Note: See page 45 for Power Packs.