

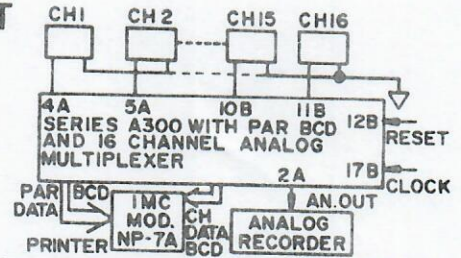
MODEL 321

HI-REL $\pm 3\frac{1}{2}$ DIGIT 16 CHANNEL ANALOG MULTIPLEXING DPM WITH TRISTATE BCD OUTPUT



FEATURES

- "3T" BCD Parallel Buffered
- Sequential Address
- Random Address
- Conditioned Analog Output
- One Instrument Can Measure 16 Signals



16 CHANNEL LOW COST DATA LOGGER

DESCRIPTION

The 321 is a 16 Channel Analog Multiplexing DPM of the single ended type meaning that all channels must have a common return at one point. Two types are available, Sequential or Random Addressing of Channel Selection. When Sequential Type is used, an External Clock Pulse steps the Internal Decoder from Channel 1 thru 16 in sequence. A Reset Pulse or Level returns the Decoder and Multiplexer to Channel "0" (Open). When Random Addressing is used, a BCD Word is used to select the appropriate channel; reset performs as in the Sequential Type. This Model as the others in this Series uses the 300 Main Frame. Refer to page

TERMINAL DESCRIPTION

Due to the number of channels offered, the 321 uses two Main Boards, the 300 Main Frame and the Analog Multiplexer Board. Due to this configuration, the Model 320 can offer Full Parallel "3T" BCD as an option; but, it must be powered by 5Vdc or External 115/230 Vac Power Supply. The 321 has two 36 Pin connectors. J1 is the Main Frame Connector and J2 is the Analog Multiplexer Connector.

J1 Connections: (Bottom)

1B (Top) +5Vdc Input; 18B, Digital Ground (5V Return) 1A (Bottom) + Signal Input from 2A of J2; 2A - Signal Input (connected internally to 18B). **Do not** allow power currents to flow on this line or **Offsets** (Ground Loops) will occur.

4A, Display Blank; 5A, Lamp Test; 6A, Display Hold (optional); 13A, -12Vdc out to 13A of J2; 14A, 1XX.X D.P.; 15A, 1X.XX D.P.; 16A, 1.XXX D.P. (connect to 18B to Light Up); 17A, +12Vdc out to 17A of J2; 18A, Sign Out (Low for +, High for -).

Pins 3 and 4B, OD1 and OD2 connect to Ground (18A) for normal operation, connect +5V to force the BCD Output to Hi Z State; 5B thru 17B, BCD out as per label (See Model 302 on page 17). **Note:** Sign Pin 18A is not tristated. When "3T" BCD is not ordered, disregard all connections pertaining to this option. Ground 12A to activate Dummy Zero.

J2 Connections: (Top)

1A +5Vdc; 18A Digital Ground; 13A (-12V) connect to 13A of J1; 17A (+12V) connect to 17A of J1; 2A + Signal Out connect to 1A of J1; 3A - Signal Out and Signal Common of all 16 Channels connect to 2A of J1; 4A-11A and 4B-11B Channels 1-16 + Inputs; 12B Reset, a Logic "0" (Ground) at this pin will clear the Decoder and force the Multiplexer to "All Open" Condition, connect to +5V for normal operation; 13B Clock, a "1" to "0" transition will advance the Multiplexer to the next channel; 14B (BCD 0); 15B (BCD 1) 16B (BCD 2); 17B (BCD 4) used as Address Inputs. If Random Model is used or as Outputs is Sequential Type is ordered.

Note: Connectors Included

SPECIFICATIONS

Linearity	0.1%
Maximum Input Voltage	$\pm 10V$
Input Impedance	10 Meg OHMS
Normal Mode Rejection	60dB @ 50-60 Hz
Clock and Reset Logic	1 Low Power TTL
No. of Channels	16
Analog Output	1mV or 1mV/Count, 1mA max.
Power Consumption	5Vdc @ 330mA
Polarity	Automatic
Zero	Automatic
Operating Temperature	-10 to +55°C
Storage Temperature	-20 to +70°C
Temperature Coefficient	$\pm 50PPM/^{\circ}C$
Input Ranges	$\pm 200mV$ and $\pm 2.0V$ F.S.
Switching Type	Break Before Make

Truth Table

	BCD	Reset	Channel
	X	0	None
+ OUT	0000	1	1
- OUT	0001	1	2
Display Blank	0010	1	3
Lamp Test	0011	1	4
Hold	0100	1	5
	0101	1	6
	0110	1	7
	0111	1	8
	1000	1	9
Dummy Zero	1001	1	10
-12V	1010	1	11
1XX.X	1011	1	12
1XX.X	0100	1	13
1XX.X	1101	1	14
+12V	1110	1	15
	1111	1	16

ORDERING INFORMATION

MODEL 321 X X X

Range/Address/3TBCD

- 0 ... 200mV/Random/No BCD
- 1 ... 2V/Random/No BCD
- 2 ... 200mV/Sequential/No BCD
- 3 ... 2V/Sequential/No BCD
- 4 ... 200mV/Random/BCD
- 5 ... 2V/Random/BCD
- 6 ... 200mV/Sequential/BCD
- 7 ... 2V/Sequential/BCD

Power

- 0 ... 5Vdc Req'd
- 1 ... Open Frame P.S.
- 2 ... Power Pack P.S.

Display

- 0 ... Standard
- 1 ... Dummy Zero

Note: See page 45 for Power Packs.