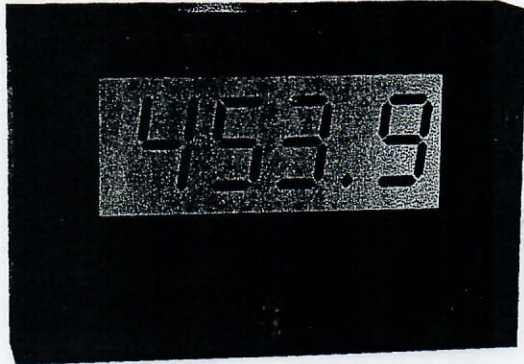


**4 DIGIT MICROPROCESSOR LCD SLAVE DISPLAY**  
**"Flat Pack" No Panel Cut Out Required**  
**(NEMA 3 or NEMA 4X)**

**MODEL**  
**546**



FLAT PACK

**Features**

- Microprocessor Compatible
- Hexadecimal or BCD Codes
- 200nS Write Pulse Width
- Direct LCD Drive
- MTBF: 80,000 Hours



SANITARY

**DESCRIPTION:** The 546 contains a 4 digit 0.5" LCD display and the industry's standard 7211A microprocessor compatible decoder driver in a very compact 2"x3"x0.5" package. The 546 accepts data in multiplexed format and displays it in either hexadecimal or code "B" format.

**MULTIPLEXED BCD INTERFACE:** The 546 has 4 BCD lines (1, 2, 4, 8) and 4 digit select (D<sub>3</sub>-D<sub>0</sub>), when one of the four D<sub>s</sub> is taken high, the data in the BCD lines is latched for that digit, if the D<sub>s</sub> is kept high continuously the BCD data is continuously updated for that digit. When the D<sub>s</sub> goes low, the data is latched until the D<sub>s</sub> goes high again. The data set-up time is 100nS, meaning that the D<sub>s</sub> can be taken high up to 100nS before the BCD data is valid. See Timing Diagram.

**μP INTERFACE:** An 8-bit I/O port from a μP is used to drive the 546's 6 bits drive, the BCD and the digit select lines. The remaining 2 bits drive the chip select (CS) lines. By tying the CS lines of the "546" together you can address 1 out of N "546" in a group, (see truth table).

**NOTE:** CS1 & CS2 are: Chip Select", lines available with "Display Font" options 2 & 3 only (see ordering information below).

**INTERFACE/DECODING/TIMING:** Figures 1-5 show the recommended interface with popular microprocessor's bus systems, as well as timing and the internal decoding.

For more detailed information, see the ICM 7211A data sheet by Maxim, Harris, or Telcom, or request it from Otek.

**HOUSING:** Otek's Flat Pack requires no panel cut out. Just drill a 10mm (3/8") Ø hole, pass the wires through, attach the provided double-sided tape (to prevent rotation), align the flat pack, tighten the nut and make the connections to the wires. No connector or tools required! No behind the panel space needed! The case is U.L. approved ABS Polycarbonate 94VO rated. Optional NEMA 4X housing for a water tight seal. Our New Sanitary case is wall, pipe or panel mount and can include 2 flat packs, please specify.

**POWER SUPPLIES:** Externally mounted. Two types are available, the "Open Frame" style accepts 120/240VAC and delivers 5VDC at up to 400mADC. The "Power Pack" is a wall plug in module available only for 120VAC input and delivers 5VDC at up to 100mADC.

**SPECIFICATIONS AT 25°C, 5VDC ±5% SUPPLY**

Input .....	TTL/CMOS Compatible
Write Pulse Width .....	200nS min.
Data Set-up Time .....	100nS min.
Data Hold Time .....	200nS
Stand-by Current .....	10μA
All 8's Current .....	2mADC
Operating/Storage Temperature .....	-10° to +60°C/-20° to +70°C
Display .....	4 Digit .5" Reflective LCD
MTBF .....	80,000 Hours
Sanitary Case .....	NEMA 4X up to 250°F Steam Clean

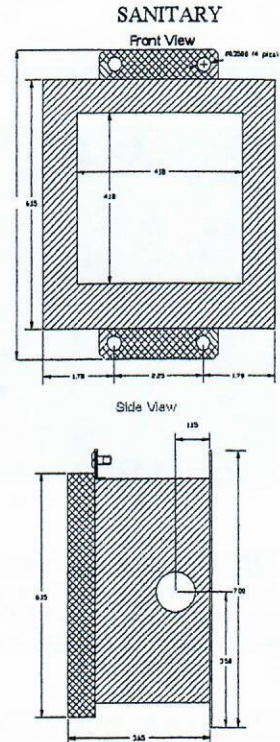
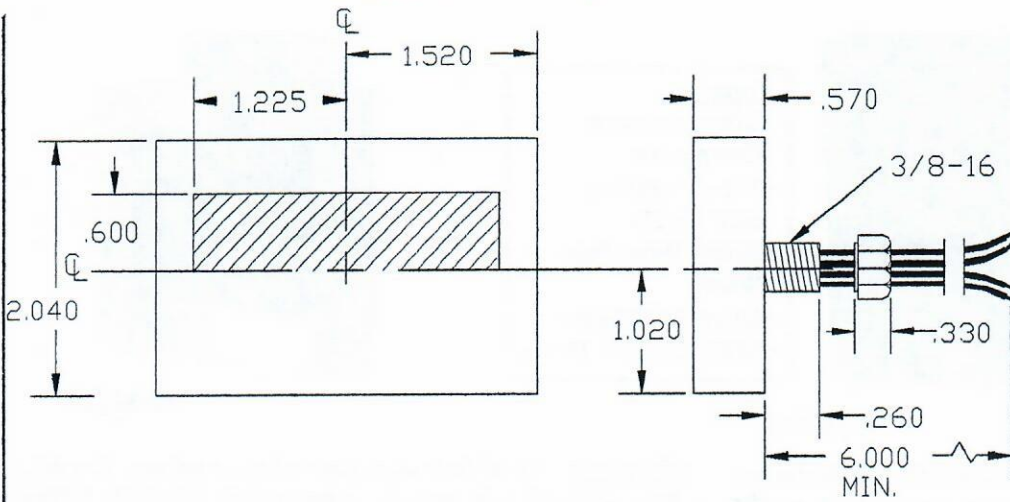
**ORDERING INFORMATION (11/1/00)**

**MODEL** 5 4 6 - - - 0

<b>DISPLAY FONT</b>	<b>POWER INPUT(1)</b>
0 ..... MUX Code "B"	0 ..... 5VDC
1 ..... MUX Hexadecimal	1 ..... Open Frame 120/240VAC
2 ..... CODE "B" uP	2 ..... Power Pack 120VAC
3 ..... "HEX" uP	
<b>HOUSING</b>	(1) See "Power Supplies" section above.
0 ..... NEMA 3	
1 ..... NEMA 4X	<b>Serial Input (7211M) on request.</b>
2 ..... SANITARY	

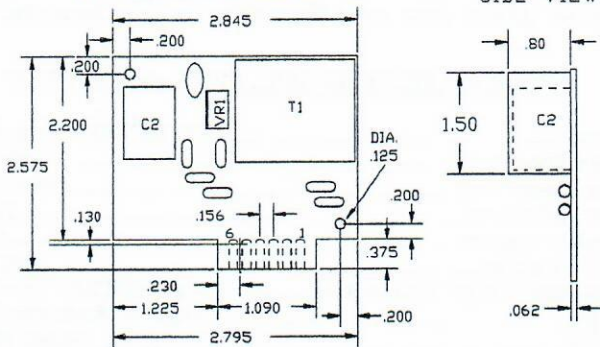
**REMOTE DISPLAYS**

546 FLAT PACK MECHANICALS & TYPICAL CONNECTIONS  
 FLAT PACK W/WIRES

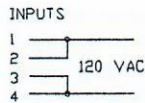


MECHANICALS FOR POWER SUPPLIES

OPEN FRAME STYLE  
 P/N 81-3110, 5VDC OUTPUT

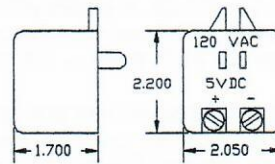


OPEN FRAME  
 POWER SUPPLY  
 TYPICAL CONNECTIONS



P/N 81-3110, 5VDC OUT

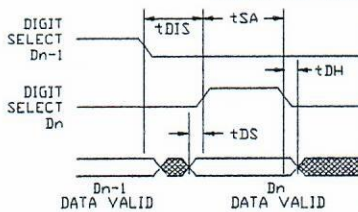
POWER PACK STYLE



ORDER P/N 75-3110 FOR 5VDC

ID3	ID1	ID2	ID0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

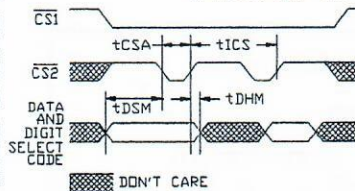
MULTIPLEXED INPUT TIMING  
 DIAGRAM AND TRUTH TABLE



F#87MC546.DWG

D1	D2	D3	D4	FUNCTION
0	0	0	0	NO CHANGE
0	0	0	1	STORE DATA IN D4 LATCH
0	0	1	0	STORE DATA IN D3 LATCH
0	1	0	0	STORE DATA IN D2 LATCH
1	0	0	0	STORE DATA IN D1 LATCH
1	1	1	1	STORE DATA IN ALL DATA LATCHES

MICROPROCESSOR INTERFACE INPUT  
 TIMING DIAGRAM AND TRUTH TABLE



DS2	DS1	CS2	CS1	FUNCTION
X	X	X	1	NO CHANGE
X	X	1	X	NO CHANGE
0	0	0	0	STORE D4 DATA
0	1	0	0	STORE D3 DATA
0	1	1	0	STORE D2 DATA
1	0	0	0	STORE D1 DATA
1	1	0	0	STORE D1 DATA
1	1	1	0	STORE D1 DATA

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