

FEATURES

- Up/Down CMOS Counter
- Dual Limits for "High-in-Low"
- 6 Digit 1/2" (13mm) Display
- Programmable Decimal Points
- Latchable Overflow
- 3T BCD TTL or CMOS
- Schmitt Trigger/Debouncer
- Relay Outputs
- Splash Proof Cover
- 1/4" DIN Aluminum Case



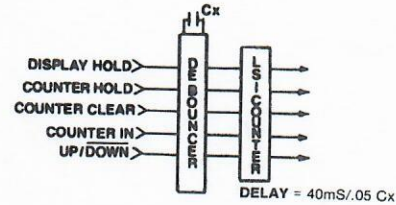
DESCRIPTION

The 810 Main Frame consists of a Mother Board where the LSI 6 Decade Up/Down Counter, IC and supporting hardware are located; a six decade Display Board with high efficiency LEDs; A Dual Limit Board where the Thumbwheel Switches and Decimal Point Selector are located and two connectors, one connector is reserved for the "3T" BCD Buffer and the other for Functional Options such as Timer, Clock, AMP-Hour, WATT-Hour, Rate Converter, Frequency, RPM, etc. In addition, an Internal Power Supply converts 115/230 VAC to 12Vdc for the high noise immunity system, Relays, when specified, are also contained on this board.

The 810 Model has dual limit setting capabilities. In these models the data from the two sets of thumbwheel switches are compared to the reading in the counter. Lights on the front panel indicate HIGHER, BETWEEN, and LOWER, with respect to the limits. Additionally, logic outputs of the three states plus high, equal, and low for each limit, and high limit latch and low limit latch are available at the edge-counter. As in the 800 models, the carry output is used to indicate an overflow condition by displaying all decimal points, except on the clock function models. Also, the latch function can be reset or disabled, just as in the 800 models.

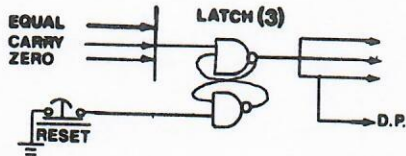
INPUT DEBOUNCER

A five-stage input debouncer interfaces mechanical contacts with the main LSI Counter. It debounces both "make" and "break" contacts. Its delay is selectable either at the factory or by field-installation of an internal capacitor. Debounce is used on the following signals; display hold, counter hold, counter clear, count input and up/down control. When the debouncer is not required, the absence of the capacitor allows the instrument to respond at its maximum input signal speed capability. (The time delay associated with the debouncing function limits the input signal speed.) When the debouncer is not used, an integral Schmitt Trigger provides hysteresis on the count input to improve noise immunity and reduce the possibility of double-triggering on slow-rising pulses.



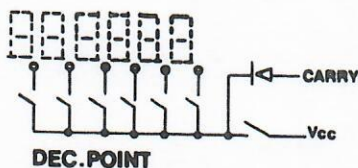
LATCH AND LATCH RESET

Latch and latch reset are standard functions on all models. They provide the user with information on when a process has exceeded a predetermined limit or maximum count — even when the equipment is unattended. It latches the equal, carry (overflow) and zero pulses converting them into levels to indicate when they have occurred. The latch function operates regardless of the direction of the count. The latch function can be disabled by leaving the "latch reset" pin disconnected. This function can be ordered in a tamper-proof configuration.



DECIMAL POINTS

Any one of six decimal points can be selected by a dip-switch on the switchboard. Only one decimal point can be on at a time. Otherwise, the LSI Chip will be damaged. An automatic all D.P. Condition indicates overflow and occurs during the 999999 → 000000 or 000000 → 999999 transition.



LEADING ZERO BLANKING (LZB)

Leading zero blanking is produced by a low state at the LZB input. Its purpose is to facilitate reading of the display and reduce power drain.



TRISTATE BCD OUTPUT

The tristate BCD output option is available for either CMOS or TTL Interfaces. It is equipped with an input disable control (memory) and three output disable lines. The latter can be grouped in 8-bit format (2 digits) or full 24-bit (6 digits) format. A Strobe Line is also available to indicate when data has been transferred to all six latches. The tristate BCD Option can be provided as a factory-installed option or it can be installed in the field at the 44-pin edge connector on the Mother Board. It terminates at the main 60-Pin Edge Connector. This option is ideal for Micro-processor and Bus System Interfaces.

